Listing of Claims

1. (Currently Amended) A tracing method, comprising:

detecting a processor mode of a processor and an application space identity (ASID) value defining an identity of a task being run on said processor;

receiving control signals defining ASID values and processor modes for which tracing is triggered;

effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values;

storing trace information in a trace memory; ~~and~~

transmitting to said trace memory synchronization information including processor mode values and ASID values; and

applying trace regeneration software to said trace information and said synchronization information to reconstruct said trace information after said task is executed on said processor.

2. (Canceled)

3. (Previously Presented) The method of claim 1, wherein an indication of said control input for said current operating state is obtained via a software-settable trace control register.

4. (Canceled)

5. (Currently Amended) The method of claim 1, wherein said processor modes comprise ~~at least one of~~ a kernel mode, a supervisor mode, a user mode, and a debug mode.

6. (Previously Presented) The method of claim 5, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on a MIPS32™ or MIPS64™ architecture specification.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Previously Presented) The method of claim 1, wherein said tracing is triggered based on G, ASID, U, K, S, DM, and X controls, wherein said G if asserted, implies that all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, S, if asserted, enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:

((G is asserted OR (ASID equals a current process application space identity value)) AND

((U is asserted AND said processor is in user mode) OR

(K is asserted AND said processor is in kernel mode) OR

(S is asserted AND said processor is in supervisor mode) OR

(DM is asserted AND said processor is in debug mode) OR

(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted))))).

11. (Currently Amended) A tracing system, comprising:

a processor core for executing instructions; and

trace generation logic that detects a processor mode of said processor core and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values;

a trace memory to store trace information and synchronization information including processor mode values and ASID values; and

trace regeneration software to ~~reconstruct~~ analyze said trace information and synchronization information after said task is executed on said processor.

12. (Canceled)

13. (Previously Presented) The tracing system of claim 11, wherein said control input is identified via a software-settable control register.

14. (Canceled)

15. (Currently Amended) The tracing system of claim 11, wherein said processor modes include ~~at least one of~~ a kernel mode, a supervisor mode, a user mode, and a debug mode.

16. (Previously Presented) The tracing system of claim 15, wherein said kernel mode, said supervisor mode, said user mode, and said debug mode are based on a MIPS32™ or MIPS64™ architecture specification.

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Previously Presented) The tracing system of claim 11, wherein said trace generation logic triggers tracing based on G, ASID, U, K, S, DM, and X controls, wherein said G if asserted, implies that all processes are to be traced, whereas if G is not asserted, trace data is processed for a current ASID value, U, if asserted, enables tracing in user mode, K, if asserted enables tracing in kernel mode, S, if asserted enables tracing in supervisor mode, DM, if asserted, enable tracing in a debug mode, and X, if asserted, enables tracing for exception and error level conditions, said controls enabling tracing when:

((G is asserted OR (ASID equals a current process application space identity value))
AND

((U is asserted AND said processor is in user mode) OR

(K is asserted AND said processor is in kernel mode) OR

(S is asserted AND said processor is in supervisor mode) OR

(DM is asserted AND said processor is in debug mode) OR

(X is asserted AND (an exception level bit is asserted OR an error level bit is asserted)))).

21. (Currently Amended) A computer program product comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions;

computer-readable program code for causing a computer to describe a trace generation logic that detects a processor mode of said processor core and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values;

computer-readable code to store trace information and synchronization information including processor mode values and ASID values;

computer-readable code to ~~reconstruct~~ analyze said trace information and said synchronization information after said task is executed on said processor; and

a computer-usable medium configured to store the computer-readable program codes.

22. (Currently Amended) A method for enabling a computer to generate a tracing system, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a processor core for executing instructions;

computer-readable program code for causing a computer to describe a trace generation logic that detects a processor mode of said processor core and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values;

computer-readable program code to store trace information and synchronization information including processor mode values and ASID values; and

computer-readable program code to ~~reconstruct~~ analyze said trace information and said synchronization information after said task is executed on said processor.

23. (Original) The method of claim 22, wherein computer-readable program code is transmitted to said computer over the Internet.

24. (Currently Amended). A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe a processor core for executing instructions;

computer-readable program code for causing a computer to describe a trace generation logic that detects a processor mode of said processor core and an application space identity (ASID) value defining an identity of a task running on said processor, said trace generation logic receiving control signals defining ASID values and processor modes for which tracing is triggered and effecting a predefined tracing control based on a logical comparison of a current processor mode and a current ASID value to said control signals, whereby tracing is triggered for selected processor modes and ASID values;

computer-readable program code to store trace information and synchronization information including processor mode values and ASID values; and

computer-readable program code to ~~reconstruct~~ analyze said trace information and said synchronization information after said task is executed on said processor.